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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,220	SWAINE, ANDREW B.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/4/05 and 5/23/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: change of address on 3/4/2005 and Amendment filed 5/23/2005.

Withdrawn Objections and Rejections

3. The Objections to claims 1-14, 16 and 18-20 set forth in the previous Office Action have been overcome via amendments to the claims. Therefore, the Objections are withdrawn by Examiner.

4. The 35 USC 101 Rejections to claims 17-21 set forth in the previous Office Action have been overcome via amendments to the claims. Therefore, the 35 USC 101 Rejections are withdrawn by Examiner.

5. The 35 USC 112 Rejections to claims 2, 19 and 20 have been overcome via amendments to the claims. Therefore, the 35 USC 112 Rejections are withdrawn by Examiner.

6. All other objections and rejections set forth in the previous Office Action and not re-stated below are withdrawn.

Specification

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested:

"APPARATUS AND METHOD FOR EFFICIENTLY INCORPORATING INSTRUCTION SET INFORMATION WITH INSTRUCTION ADDRESSES IN TRACE DATA"

Maintained Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 21 recites the limitation "A computer program product carrying a computer program for controlling an apparatus in accordance with the method of claim 17." This limitation is indefinite, as it is unclear to the examiner if this claim was intended to be an independent claim, as claim 17 is a method claim and this limitation is directed toward a computer readable medium (and before the amendment a computer program product).

New Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Advanced RISC Machines, "Embedded Trace Macrocell (Rev 0/0a): Specification", hereinafter ARM.

16. Regarding claim 1, ARM has taught an apparatus for processing data, said apparatus comprising:

a. A processing circuit [ARM, Figure 1-1, Page 1-3] for executing processing instructions from any of a plurality of instruction sets of processing instructions [ARM and Thumb, Section 1.1.1, Page 1-4], each processing instruction being specified by an instruction address identifying that processing instruction's location in memory [It is inherent that instructions have an associated address in memory]

b. The instruction address having a predetermined number of bits irrespective of the instruction set to which the associated processing instruction belongs: [A "full" address is 32-bits, which is a predetermined number of bits, irrespective of the instruction set. Page 2-10, first line.]

c. But a different number of most significant instruction address bits needing to be specified in the instruction address to uniquely identify processing instructions

in different instruction sets [Section 2.5.1, Page 2-8, 5th paragraph, bit 1 of the address for ARM instructions is ignored, therefore, more bits are required to uniquely identify the Thumb instructions than the ARM instructions]; and

d. Encoding logic for encoding at least one instruction address with an indication of the instruction set corresponding to that instruction to generate an n-bit encoded instruction address [Section 2.5.1, Page 2-8, 4th paragraph, the logic that encoded bit 0 of the instruction address is inherent],

e. The encoding logic being arranged to perform the encoding by performing a computation equivalent to removing any least significant bits not forming the instruction address bits needing to be specified [The least significant bit (LSB, bit 0) of the ARM and Thumb addresses is replaced by an indication of the type of instruction that address corresponds to. (LOW for ARM, HIGH for Thumb) The act of replacing a LSB is a "computation equivalent to removing". Also, the second LSB (bit 1) is "traced as zero for ARM instruction[s]". Therefore, the second LSB (bit 1) is replaced with a zero, which is a "computation equivalent to removing". (Page 2-6, section 2.5.1)].

f. And extending the specified instruction address bits to n-bits by appending a pattern of bits to the specified instruction address bits, the number of least significant bits removed and the pattern of bits prepended being dependent on the instruction set corresponding to that instruction: (The 2 LSBs of an ARM instruction are replaced with a '00', which indicates the type of instruction. The LSB of Thumb instructions is replaced with a "1". Therefore, the number of LSBs

removed and the pattern of bits are dependent on the type of instruction. (Page 2-6, section 2.5.1)

17. However, ARM teaches *appending* the pattern of bits to the instruction address instead of *prepending* the pattern of bits.

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to *prepend* the pattern of bits instead of *append,* since it has been held shifting the position of parts is obvious. (In re Japikse; 181 F.2d 1019, 86 USPQ 70 (CCPA 1950)*]*.

19. Examiner also takes Official Notice that when transferring data, it is well known in the art to place information about data that is about to be transferred at the beginning of data to be transferred (e.g., a header), so that a receiver will know information about the data it is about to receive, before it actually receives the data, and then can take the appropriate action.

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to prepend the pattern of bits instead of append them, since Examiner takes Official Notice place information about data about to be transferred at the beginning of data to be transferred.

21. Regarding claim 2, ARM, has taught the apparatus as claimed in claim 1, wherein the ARM instruction addresses have a “00” prepended to it and the Thumb instruction addresses have a “1” prepended. Therefore, ARM does not teach wherein for each instruction set a first pattern of bits prepended to the specified instruction address bits of an instruction address from that instruction set is related to a second

pattern of bits prepended to the specified instruction address bits of instruction addresses of different instruction sets by shifting the first pattern of bits.

22. However, the only difference between the prior art (ARM) and claim is that the ARM instruction has a "0" for bit 1 [ARM teaches "bit 1 of the address will be traced as zero"]. If bit 1 was set to "1", then the ARM instruction address would have a second pattern, which is related by shifting the first pattern. To further explain, the Thumb instruction address pattern is a "1", while the ARM instruction address pattern is "00". However, shifting the Thumb pattern to the left by one bit would create a pattern "10" or "1x" (x representing don't care). Therefore, if the ARM address pattern was "10" instead of "00", it would be related by a shift.

23. Although ARM doesn't specifically disclose bit 1 being set to "1", and therefore the first and second bit patterns are not related by shifting, such limitations are merely a matter of design choice and would have been obvious in the system of ARM. ARM instruction addresses have a zero for bit 1 [ARM teaches "bit 1 of the address will be traced as zero", page 2-6, section 2.5.1], the zero is an arbitrary value. The limitations in claim 2 do not define a patentably distinct invention over that in ARM since the difference is merely a bit being set to zero versus. a bit being set to one, which is inconsequential for the invention as a whole and presents no new or unexpected results. Therefore, to have bit 1 set to "1" would have been a matter of obvious design choice to one of ordinary skill in the art.

24. Regarding claim 3, ARM, has taught the apparatus as claimed in claim 1, wherein the encoding logic is arranged to perform the encoding by performing a

computation equivalent to generating an intermediate value by pre-pending a predetermined pattern of bits to the specified instruction address bits of the instruction address and then selecting as the encoded instruction address n bits from the intermediate value [Section 2.5.1, Page 2-8, 4th paragraph, the indication is prepended to the instruction address, creating an intermediate value, then all bits are selected from the intermediate value].

25. Regarding claim 4, ARM, has taught the apparatus as claimed in claim 1, further comprising compression logic for compressing a said encoded instruction address by performing a computation equivalent to partitioning that encoded instruction address into a plurality of x-bit sections, comparing each x-bit section with the corresponding x-bit section of a preceding encoded instruction address and outputting as a compressed encoded instruction address the most significant x-bit section that differs from the corresponding x-bit section of the preceding encoded instruction address, along with any less significant x-bit sections [Section 2.5.1, Compressed branch address packet structure, page 2-9, 4th paragraph].

26. Regarding claim 5, ARM has taught the apparatus as claimed in claim 4, wherein the compression logic is arranged to associate with each x-bit section to be output from the compression logic a flag to indicate whether that x-bit section is the last x-bit section being output as the compressed encoded instruction address [Section 2.5.1, Compressed branch address packet structure, page 2-9, 3rd paragraph].

27. Regarding claim 6, ARM has taught the apparatus as claimed in claim 5, wherein if a plurality of x-bit sections are to be output from the compression logic, the plurality of

x-bit sections are output sequentially starting with the least significant x-bit section [Section 2.5.1, Compressed branch address packet structure, page 2-10, the flag bit indicates if there are additional packets in the address stream, the most significant packet has an indication that there are no more packets, meaning the least significant packets are sent first].

28. Regarding claim 7, ARM has taught the apparatus as claimed in claim 5, wherein the compression logic is further arranged to expand to y bits each x-bit section to be output from the compression logic, with the most significant y-x bits containing the flag [Section 2.5.1, Compressed branch address packet structure, page 2-9, the flag bit is appended to the address packets as bit 7 (MSB), making the packets 8-bits in length].

29. Regarding claim 8, ARM has taught the apparatus as claimed in claim 7, wherein the flag is a single bit [Section 2.5.1, Compressed branch address packet structure, page 2-9].

30. Regarding claim 9, ARM has taught the apparatus as claimed in claim 8, wherein y is 8 and x is 7 [Section 2.5.1, Compressed branch address packet structure, page 2-9, the compressed packet length is 8 bits, including the flag bit, therefore, the encoded packet length was 7 bits before the flag bit was appended to the compressed packet to make it 8 bits].

31. Regarding claim 10, ARM has taught the apparatus as claimed in claim 1, but has not explicitly taught wherein the encoding logic comprises an n-bit selector logic unit for receiving the intermediate value and an identifier signal identifying the instruction set associated with the instruction address contained within the intermediate value, the n-bit

selector being arranged to output a predetermined n-bits of the intermediate value dependent on the identifier signal.

32. The apparatus of ARM attempts to limit the amount of data saved and sent for tracing. Providing a selector circuit in the encoding logic that only selects a subset of bits from the intermediate signal would allow the instruction address to be compressed even further. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the apparatus of ARM to include a selector circuit in the encoder logic in order to allow for only a subset of bits to be sent to the compression logic.

33. Regarding claim 11, ARM has taught the apparatus as claimed in claim 4, wherein the compression logic comprises a plurality of comparators, each comparator being arranged to receive a corresponding x-bit section of the encoded instruction address, and including temporary storage for storing the corresponding x-bit section of the preceding encoded instruction address, the comparator being arranged to compare the two x-bit sections and to generate a difference signal which is set when the two x-bit sections are different [Section 2.5.1, Compressed branch address packet structure, page 2-9. The compression logic "registers the last branch address that it has broadcast" and compares the preceding branch address to the current address in sections, therefore, it is inherent that there are a plurality of comparators to compare the individual sections. It is inherent that a difference signal be present in order to indicate that the flag bit should or should not be set.].

34. Regarding claim 12, ARM has taught the apparatus as claimed in claim 11, wherein the compression logic further comprises a flag generator logic arranged to

generate for each x-bit section to be output from the compression logic a flag based on predetermined combinations of the difference signals generated by the plurality of comparators, such that a flag for a particular x-bit section is set if a more significant x-bit section is also to be output [Section 2.5.1, Compressed branch address packet structure, page 2-9. The packets are sent in sequential order with the least significant packet being first. The flag is only set if there are additional packets in the address stream. Therefore, it is inherent that there is flag generator logic to set the flag according to different combinations of the difference signals.].

35. Regarding claim 13, ARM has taught the apparatus as claimed in claim 12, wherein the compression logic further comprises an output generator for generating the compressed encoded instruction address by pre-pending to each x-bit section to be output its corresponding flag, thereby generating as the output compressed encoded instruction address a sequence of y-bit sections [Section 2.5.1, Compressed branch address packet structure, page 2-9. It is inherent that there is an output generator logic to prepend the flag bit to the address packets.].

36. Regarding claim 14, ARM has taught the apparatus as claimed in claim 4, wherein the encoding logic and compression logic are provided within a trace module used to trace activities of the processing circuit [Section 2.2, Structure of the trace port, page 2-3, the device is an Embedded Trace Macrocell used for tracing the activities of the processor].

37. Regarding claim 15, given the similarities between the claims, the arguments as stated for claim 1 are also applicable to claim 15.

38. Regarding claim 16, given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 16.

39. Regarding claim 17, given the similarities between the claims, the arguments as stated for claims 1 and 2 are also applicable to claim 17.

40. Regarding claim 18, given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 18.

41. Regarding claim 19, ARM has taught the method according to claim 18, but is silent on the method further comprising the steps of decompressing the compressed, encoded instruction address.

42. However, examiner takes OFFICIAL NOTICE that decompressing the compressed, encoded instruction address would be accomplished by reversing the process of compression. The compression method determines the packets that are different from the previous instruction address, sets the appropriate flag bits and sends only the difference packets. Reversing the process would comprise the steps of determining the number of packets sent (using the flag bits), and replacing the missing packets (the total number of packets should be five) with the corresponding packets of the previous instruction address. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the method ARM to further comprise the steps decompressing the compressed, encoded instruction address by reversing the process of compression.

43. Regarding claim 20, ARM has taught the method as claimed in claim 19, but is silent on the method further comprising the step of decoding the encoded instruction address

by performing a computation equivalent to determining from the predetermined pattern of bits the instruction set to which the instruction address relates, and removing the predetermined pattern of bits to yield the specified instruction address bits.

44. However, the examiner takes OFFICIAL NOTICE that decoding the encoded instruction address would be accomplished by removing the prepended instruction set indication bits, yielding the instruction address. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the method of ARM to further comprise the steps of decoding the encoded instruction address by reversing the process of encoding.

45. Regarding claim 21, ARM, has taught a computer program product carrying a computer program for controlling an apparatus in accordance with the method of claim 17 [It is inherent that there is a computer program for controlling an apparatus in accordance with the method claim 17, which must be contained on a computer program product for it to be statutory.].

46. Regarding claim 22, given the similarities between the claim 14, the arguments as stated for claim 14 are also applicable to claim 22.

Response to Arguments

12. Applicants arguments filed on 5/23/2005 have been fully considered but they are not persuasive.

13. Applicant argues the novelty/rejection of claims 1, 15 and 17.

"[T]he examiner is incorrect in arguing that the encoding logic described in the earlier ARM citation describes a technique where a bit is prepended to the specified instruction

address bits, since in accordance with the Arm citation, it is the least significant bit and not the most significant bit that is subjected to the encoding."

14. These arguments are not found persuasive for the following reasons:

a. To clarify, applicant's attention is directed towards the new 35 USC 103 rejections to claims 1, 15 and 17 above where this limitation is addressed.

Examiner agrees that the ARM reference does not teach *prepending* the encoded bits, the ARM reference teaches *appending* the encoded bits.

However, as stated above, it would have been obvious to *prepend* the bits instead of *append* the bits.

15. Applicant argues the novelty/rejection of claims 1, 15 and 17.

"The ARM citation technique also neither removes any least significant bits not forming the instruction address bits needing to be specified nor extends the specified instruction address bits to n-bits by prepending a pattern of bits to the specific instruction address bits."

16. These arguments are not found persuasive for the following reasons:

b. To clarify, applicant's attention is directed towards the 35 USC rejections to claims 1, 15 and 17 above. The ARM teaches removing the least significant bits of the instruction address that are not needed to specify the address. The two LSBs of ARM instruction addresses are replaced with "00". The LSB of Thumb instruction addresses is replaced with a "1". The replacing of the two LSBs of ARM instruction addresses and the one LSB of Thumb instruction addresses is a *removal* of LSBs. Also, since the unneeded LSBs are removed and since it would have been obvious to prepend the encoded bits as stated above, the instruction address is extended to n-bits.

17. Applicant argues the novelty/rejection of claims 1, 15 and 17.

"But as defined in claim 1, the claimed encoding logic generates an encoded form of instruction address, which is not used by the processing circuit [to?] address an instruction, but which does contain sufficient information to enable the instruction address to be derived and also provides an indication of the type of instruction set."

"By performing a computation equivalent to removing any least significant bits not forming the instruction address bits needing to be specified , and then extending the remaining specified instruction address bits to n-bits by prepending a pattern of bits to the specified instruction address bits, the bit position of each specified instruction address bit is shifted. No such encoding technique is disclosed in Nevill."

18. These arguments are not found persuasive for the following reasons:

c. To clarify, applicant's attention is directed towards the new 35 USC 103 rejections to claims 1, 15 and 17 above. Nevill is not used in the rejections, therefore the arguments relating to the teachings (or lack of teachings) of Nevill are moot.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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